

traversed and reconsideration of the claims is respectfully requested in view of the following remarks.

The rejection of claims 1, 3, 4, and 15 under 35 U.S.C. § 102(b) as being anticipated by Nomura et al. is respectfully traversed and reconsideration is respectfully requested.

While claims 1, 3, 4, and 15 were rejected under 35 U.S.C. § 102(b), Applicants respectfully submit that Nomura et al., having an issue date of May 22, 2001, was not patented more than one year prior to the filing date of the present application, i.e., September 22, 2000. Accordingly, Applicants respectfully submit that Nomura et al. is not available as prior art under 35 U.S.C. § 102(b).

Even assuming that Nomura et al. was available as prior art under 35 U.S.C. § 102(b), claim 1 is allowable over the cited references in that claim 1 recites a combination of elements including, for example, “resetting each liquid crystal cell of the liquid crystal display device simultaneously”. None of the cited references, including Nomura et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 1 and claims 2 and 3, which depend therefrom are allowable over the cited references.

The Examiner cites Nomura et al. as showing “resetting each liquid crystal cell of the liquid crystal display device simultaneously (col. 28, lines 54-67).” Applicants respectfully submit, however, Nomura et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 1. For example, Applicants respectfully submit Nomura et al. states at column 28, lines 61-66 “...the voltage settings of the second example enable the simultaneous implementation of a large voltage of over 20V and a small bias voltage in the region of 1V, while keeping the voltage values close with each other and

having axis symmetry of the zero-potential...” The Examiners’ aforementioned citation Nomura et al. is actually a portion of a disclosure related to an embodiment illustrated in Figures 32A and 32B. In reference to Figures 32A and 32B, Nomura et al. states in column 27, lines 63-65 “Scan signals Y_n and Y_{n+1} indicate the scan signals supplied to the n th and the $(n+1)$ th row electrodes, respectively.” and at column 28, lines 17-20 “Scan signal Y_{n+1} is the waveform of the next row’s scan signal. It differs from scan signal Y_n in that each of reset period T_1 , delay period T_2 , and selection period T_3 are shifted by the time $(1/H)$ required for one line.” Accordingly, Applicants respectfully submit Nomura et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 1.

Claim 4 is allowable over the cited references in that claim 4 recites a combination of elements including, for example, “wherein a reset voltage is applied to all liquid crystal cells of the liquid crystal display device to reset the liquid crystal display device”. None of the cited references, including Nomura et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 4 and claims 5-8, which depend therefrom are allowable over the cited references.

The Examiner cites Nomura et al. as showing “wherein a reset voltage is applied to all liquid crystal cells of the liquid crystal display device to reset the liquid crystal display device (col. 3, lines 16-22).” Applicants respectfully submit, however, Nomura et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 4. For example, Applicants respectfully submit Nomura et al. states at column 3, lines 45-54 “When the method of the present invention is applied to driving a matrix liquid crystal

device, a difference signal $Y_n - X_m$... is made to include, ...a reset period T1 that is set before selection period T3, and a delay period T2 that is set between reset period T1 and selection period T3, as shown in FIGS. 8A-8D. In this case, row electrode signal Y_n is at a reset potential V_r during reset period T1...” Similar arguments presented above with respect to claim 1 is also applicable to claim 4. Accordingly, Applicants respectfully submit Nomura et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 4.

Claim 15 is allowable over the cited references in that claim 15 recites a combination of elements including, for example, “means for simultaneously resetting all of the liquid crystal cells”. None of the cited references, including Nomura et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 15 and claims 16 and 17, which depend therefrom are allowable over the cited references. Similar arguments presented above with respect to claim 1 is also applicable to claim 15.

The rejection of claims 12-14 under 35 U.S.C. § 103(a) as being unpatentable over Nomura et al. is respectfully traversed and reconsideration is respectfully requested.

Claim 12 is allowable over the cited references in that claim 12 recites a combination of elements including, for example, “logical OR gates for performing a logical OR operation of an input reset signal and each gate driving signal from the shift register”. None of the cited references, including Nomura et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 12 and claims 13 and 14, which depend therefrom are allowable over the cited references.

The Examiner cites Nomura et al. as teaching in Figure 38 “a shift register (111) for generating sequential gate driving signals; logical OR gates (64) for performing a logical OR operation of an input reset signal and each gate driving signal from the shift register; and level shifters (114).” Applicants respectfully submit, however, that the elements within the Examiners’ aforementioned citation of Nomura et al. are disclosed in separate, unrelated, embodiments. For example, Nomura et al. states at column 31, lines 36-54, “A block diagram of a drive circuit for scan signal electrodes (row electrodes), for implementing the drive methods of the sixteenth to the twenty-first embodiments, is shown in FIG. 38. ...In FIG. 38, ...Signals RE and S are input to shift registers 111 and 112, respectively. ...A 2-to-4 decoder 113 identifies three register output states of signals RE and S ... and outputs them through a level shifter 114 to a Y driver 115.” Additionally, Applicants respectfully submit it is well known in the art that 2-to-4 decoders such as those disclosed by Nomura et al. do not include any logical OR gates. In the Ninth Embodiment, Nomura et al. states at column 19, lines 25-44, “FIG. 20 shows a circuit that outputs a scan signal Yn... To shape scan signal Yn waveform, the scan signal drive circuitry shown in FIG. 20 has a first analog switch 70...A monostable circuit 40, and various logic gates 50-55 and 60-64 are used to drive these analog switches...” Accordingly, Applicants respectfully submit Nomura et al. does not disclose at least the aforementioned combination of elements with respect to independent claim 12.

The rejection of claims 2, 5-11, 16, and 17 under 35 U.S.C. § 103(a) as being unpatentable over Nomura et al. in view of Oda et al. is respectfully traversed and reconsideration is respectfully requested.

Claim 2 includes all of the limitations of claim 1 as discussed above, and Nomura et al. fails to teach or suggest at least the features of independent claim 1 as recited above.

Similarly, Oda et al. fails to cure the deficiencies of Nomura et al. Accordingly, Applicants respectfully submit that the Examiner has not established a *prima facie* case of obviousness regarding claim 2, as above.

Claims 5-8 include all of the limitations of claim 4 as discussed above, and Nomura et al. fails to teach or suggest at least the features of independent claim 4 as recited above. Similarly, Oda et al. fails to cure the deficiencies of Nomura et al. Accordingly, Applicants respectfully submit that the Examiner has not established a *prima facie* case of obviousness regarding claims 5-8, as above.

Claim 9 is allowable over the cited references in that claim 9 recites a combination of elements including, for example, “voltage selecting means for selecting...a normal common voltage to be applied... in an interval when a data voltage is charged and maintained in all liquid crystal cells of the liquid crystal display, and for selecting... a reset voltage less than the normal common voltage to be applied to the common electrode in a reset interval.” None of the cited references, including Nomura et al. or Oda et al., singly or in combination, teaches or suggests at least these features of the claimed invention.

Claim 10 is allowable over the cited references in that claim 10 recites a combination of elements including, for example, “a voltage amplifier for amplifying an input control signal having a specific logical state only in a reset interval when liquid crystal cells of the liquid crystal display device are reset...” None of the cited references, including Nomura et al. or Oda et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicant respectfully submits that independent claim 10 and claim 11, which depends therefrom are allowable over the cited references.

Claims 16 and 17 include all of the limitations of claim 15 as discussed above, and Nomura et al. fails to teach or suggest at least the features of independent claim 15 as recited above. Similarly, Oda et al. fails to cure the deficiencies of Nomura et al. Accordingly, Applicants respectfully submit that the Examiner has not established a *prima facie* case of obviousness regarding claims 16 and 17, as above.

Applicant believes the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136. Please credit any overpayment to deposit Account No. 50-0911.

Respectfully submitted,

MCKENNA LONG & ALDRIDGE, LLP

Date: July 29, 2002

By



Kurt M. Eaton
Registration No: P-51,640

Rebecca Goldman Rudich
Registration No: 41,876

1900 K Street, N.W.
Washington, D.C. 20006
Telephone No.: (202) 496-7500
Facsimile No.: (202) 496-7756



30827

PATENT TRADEMARK OFFICE